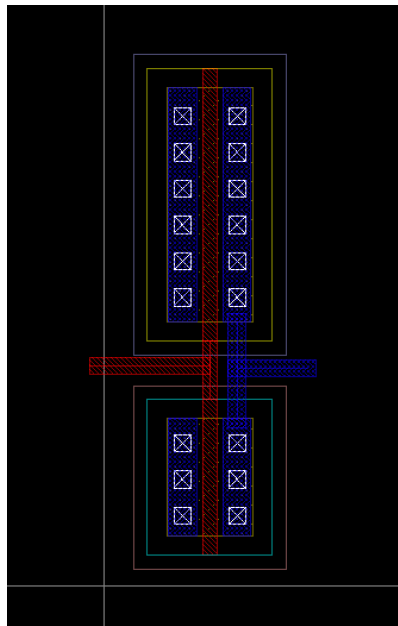


Glade training part 2 - lab

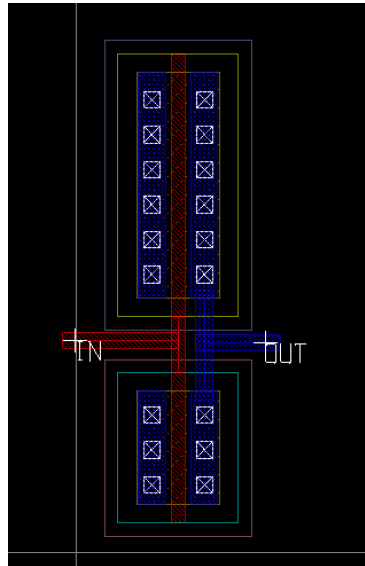
- Start in the training directory
 - `cd glade_training/Part2`
- Make sure your PYTHONPATH includes the location of the training directory Part2:
 - `PYTHONPATH=.:glade_training/Part2:$GLADE_HOME:$PYTHONPATH`
- Open Glade from the cmd line or icon
- Create a new library
 - File->New Library
 - Give the library a name e.g. part2
 - Using the file chooser icon, select the techfile 'example.tch'
 - Press OK. The library is created
- Create a new cellView
 - In the library browser, RMB on the library name you created
 - Select 'Create CellView'
 - Set the Cell Name to 'inv'
 - Press OK. The cellView is created.
- Import the PCells into the library
 - File->New Cell
 - Click on 'CellView is a PCell'
 - Use the file chooser to select the PCell script 'nch.py'
 - Press OK. The PCell master layout will be opened.
 - Repeat for the PCell 'pch.py'
 - Close the 'nch layout' and 'pch layout' cellViews

- Place an instance of an nmos device in the 'inv layout' cellView
 - Create->Instance ('I' bindkey)
 - If the Create Instance dialog does not show, open it using F3
 - Choose the cell name as 'nch'
 - Left click to place the instance.
- Place an instance of a pmos device using the same method.
- Select the pmos instance (LMB click) and query its properties (q bindkey, select Properties tab)
- Change it's width to 2.2e-06 (2.2um) and click OK.
 - Note how the PCell instance width is changed.
- Now align the instances.
 - Edit->Align or 'a' bindkey
 - Choose align horizontally
 - Click on Set Reference Object button then click on one of the instances, then the other.
 - The instances are aligned to the same X axis position.
- Experiment with moving an instance.
 - Select an instance and use Edit->Move ('m' bindkey)
 - F3 to show the dialog if not already shown
 - Try rotating, setting snap mode etc.
 - ESC key quits the cmd
- Now connect the device poly gates together
 - Choose layer 'polyg' by selecting it in the LSW.
 - Draw a path (Create->Path or 'p' bindkey) to add a poly strap between the gates.
 - Note the default path width is set from the minimum in the techfile.
 - Double click or press enter to end the path.

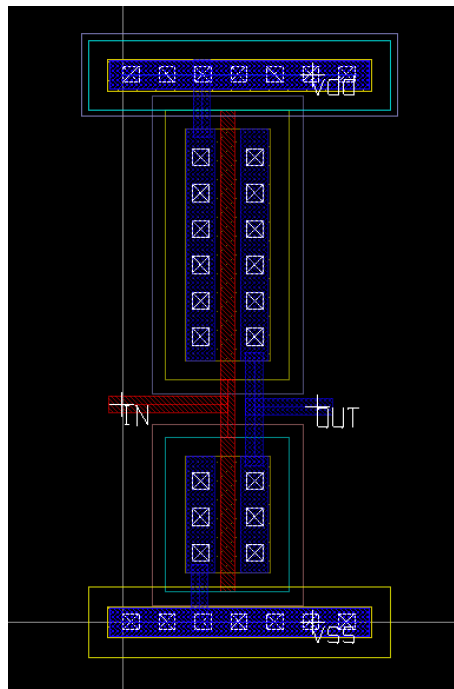
- You can connect up the source/drain metal pins by selecting metal1 in the LSW and then drawing paths/rectangles/polygons to join them.
 - You should be able to create something like the following:



- Add text labels
 - Select the potxt layer in the LSW
 - Using the Create Label command, set the name to IN and the height to 0.2. Position the label over the poly shape.
 - Select the m1txt layer in the LSW
 - Using the Create Label command, set the name to OUT and the height to 0.2. Position the label over the output metal1 shape.
- The layout should look like this:



- Now add a MPP for the VDD and VSS power rails.
 - Use Create->MPP and set the name to nguard and the net to vdd
 - Draw a path from the top left to top right and double click or use return to finish the path
 - Use Create->MPP and set the name to pguard and the net to vss
 - Draw a path from the bottom left to bottom right.
- Add power and ground labels
 - Select the m1txt layer in the LSW
 - Using the Create Label command, set the name to vss and the height to 0.2. Position the label over the lower guard ring shape.
 - Do the same to create a vdd label over the upper guard ring shape.
- Add a strap from the nmos source to the ground rail and the pmos source to the vdd rail.
- You should end up with a layout something like this:



This concludes the lab session for Part 2.